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Substitute for form 1449A/PTO		Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>		Application Number	09/892,566
JCP		Filing Date	June 28, 2001
Sheet		First Named Inventor	SOLOMON et al
1		Group Art Unit	2188
of		Examiner Name	G.J. Portka
1		Attorney Docket Number	2207/10607

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>2</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS		
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

Examiner Signature	GARY J. PORTKA	Date Considered	1/9/05
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**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		<i>Filing Date</i> June 28,2001	<i>First Named Inventor</i> B. Solomon et al.
		<i>Art Unit</i> 2188	<i>Examiner Name</i> Gary J. Portka
Sheet 1 of 2		<i>Attorney Docket Number</i> 02207/10607	

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## U.S. PATENT DOCUMENTS

Examiner Initials * <i>GJP</i>	Cite No. ↑	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number – Kind Code <sup>2</sup> (if known)			
		US-6,507,921	01-14-03	Buser et al.	
		US- 6,351,844	02-2002	Bala	
		US- 6,339,822	01-15-02	Miller	
		US- 6,279,103	08-21-01	Warren	
		US- 6,233,678	05-15-01	Bala	
		US- 6,216,200	04-10-01	Yeager	
		US- 6,189,140	02-13-01	Madduri	
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		US- 5,924,092	07-1999	Johnson	
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		US- 4,575,814	03-11-86	Brooks, Jr., et al.	
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## FOREIGN PATENT DOCUMENTS

Examiner Signature	GARY J. PORTKA	Date Considered	1/9/05
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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

## Complete if Known

Application Number	09/892,566
Filing Date	June 28,2001
First Named Inventor	B. Solomon et al.
Art Unit	2188
Examiner Name	Gary J. Portka
Attorney Docket Number	02207/10607

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## NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
GJP		Conte et al, "Optimization of Instruction Fetch Mechanisms for High Issue Rates," <i>Proceedings of the 22nd Annual Int'l. Symposium on Computer Architecture</i> , June 22-24, 1995, Santa Margherita Ligure, Italy, pp. 333-344	
		Dutta et al, "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors," <i>Proceedings of the 28<sup>th</sup> Int'l. Symposium on Microarchitecture</i> , Nov. 29-Dec. 1, 1995, Ann Arbor, MI, pp. 258-263.	
		Hennessy et al., <i>Computer Organization and Design: the hardware/software interface</i> , 2 <sup>nd</sup> Edition, Morgan Kaufmann Publishers, San Francisco, CA, 1998, p. 570.	
		Johnson, Mike, <i>Superscalar Microprocessor Design</i> , PTR Prentice-Hall, Englewood Cliffs, New Jersey, 1991, Chapter 10, pages 177-202.	
		Jourdan et al, "eXtended Block Cache," Intel Corporation, Intel Israel, Haifa, 31015, Israel, pages 1-10.	
		McFarling, Scott, "Combining Branch Predictors," June 1993, WRL Technical Note TN-36, Digital Western Research Laboratory, Palo Alto, CA, 25 pp.	
		Michaud et al, "Exploring Instruction-Fetch Bandwidth Requirement in Wide-Issue Superscalar Processors," <i>Proceedings of the 1999 Int'l. Conference on Parallel Architectures and Compilation Techniques</i> , Oct. 12-16, 1999, Newport Beach, CA, pp. 2-10.	
		Patel et al, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing," <i>Proceedings of the 25<sup>th</sup> Annual Int'l. Symposium on Computer Architecture</i> , June 27-July 1, 1998, Barcelona, Spain, pp. 262-271.	
		Reinman et al, "A Scalable Front-End Architecture for Fast Instruction Delivery," <i>Proceedings of the 26<sup>th</sup> Int'l. Symposium on Computer Architecture</i> , May 2-4, 1999, Atlanta, GA, pp. 234-245.	
		Rotenberg et al, "Trace Processors," <i>Proceedings of 30<sup>th</sup> Annual IEEE/ACM International Symposium on Microarchitecture</i> , December 1, 1997, Research Triangle Park, NC, pp. 138-148.	
		Seznec et al, "Multiple-Block Ahead Branch Predictors," <i>Proceedings of the 7<sup>th</sup> Int'l. Conference on Architectural Support for Programming Languages and Operating Systems</i> , Oct. 1-4, 1996, Cambridge, MA, pp. 116-127.	
GJP		Yeh et al, "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache," <i>Proceedings of the 7<sup>th</sup> Int'l. Conference on Supercomputing</i> , July 1993, Tokyo, Japan, pp. 67-76.	

Examiner Signature

GARY J. PORTKA

Date Considered

1/9/05

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